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**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA 533 003**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech- II Semester**

Specialization: VLSID/VLSISD

COURSE STRUCTURE

Code	Name of the Subject	L	P	C	INT	EXT	TOTAL
Core							
	1. Algorithms for VLSI Design Automation	4	-	8	40	60	100
	2. Low Power VLSI Design	4	-	8	40	60	100
	3. DSP Processors & Architecture	4	-	8	40	60	100
	4. Design of Fault Tolerant Systems	4	-	8	40	60	100
Elective III							
	1. Embedded and Real Time Systems	4	-	8	40	60	100
	2. System Modeling & Simulation						
Elective IV							
	1. CPLD and FPGA Architecture and Applications	4	-	8	40	60	100
	2. Advanced Microcontrollers and Processors						
Laboratory							
	Mixed Signal Simulation Laboratory	-	4	4	40	60	100

ALGORITHMS FOR VLSI DESIGN AUTOMATION

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

Layout Compaction, Placement, Floorplanning and Routing Problems, Concepts and Algorithms

UNIT IV

MODELLING AND SIMULATION: Gate Level Modelling and Simulation, Switch level modeling and simulation

UNIT V

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary – Decision diagram, Two – Level Logic Synthesis.

UNIT VI

HIGH LEVEL SYNTHESIS: Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations.

UNIT VII

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's partitioning and Routing for segmented and staggered models.

UNIT VIII

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM's.

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, John wiley & Sons (Asia) Pvt.Ltd. 1999.
2. Algorithms for VLSI Physical Design Automation, 3rd edition, Naveed Sherwani, Springer International Edition, 2005

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993
2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition, 1998

LOW POWER VLSI DESIGN

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

MOS/BiCMOS PROCESSES : Bi CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT III

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes ,SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT IV

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models.

UNIT V

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid-mode environment.

UNIT VI

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates. Performance evaluation

UNIT VII

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced BiCMOS Digital circuits. ESD-free Bi CMOS , Digital circuit operation and comparative Evaluation.

UNIT VIII

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

REFERENCES

1. Digital Integrated circuits , J.Rabaey PH. N.J 1996
2. CMOS Digital ICs sung-moKang and yusuf leblebici 3rd edition TMH2003(chapter 11)
3. VLSI DSP systems , Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

DSP PROCESSORS AND ARCHITECTURES

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV

EXECUTION CONTROL AND PIPELINING

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT V

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT VI

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT VII

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

DESIGN OF FAULT TOLERANT SYSTEMS

UNIT I

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and Meantime between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

UNIT II

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), SMR Configuration, Use of error correcting code, Time redundancy and software redundancy.

UNIT III

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

UNIT IV

FAIL SAFE DESIGN: Strongly fault secure circuits, fail-safe design of sequential circuits using partition theory and Berger code, totally self-checking PLA design.

UNIT V

DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable design.

UNIT VI

Theory and operation of LFSR, LFSR as Signature analyzer, Multiple-input Signature Register.

UNIT VII

DESIGN FOR TESTABILITY FOR SEQUENTIAL CIRCUITS: Controllability and observability by means of scan register, Storage cells for scan design, classic scan design, Level Sensitive Scan Design (LSSD).

UNIT VIII

BUILT IN SELF TEST: BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture.

TEXT BOOKS:

1. Parag K. Lala – “Fault Tolerant & Fault Testable Hardware Design” (PHI)

2. M. Abramovili, M.A. Breues, A. D. Friedman – “Digital Systems Testing and Testable Design” Jaico publications.

EMBEDDED AND REAL TIME SYSTEMS

UNIT I: INTRODUCTION

Embedded systems over view, design challenges, processor technology, Design technology, Trade-offs. Single purpose processors RT-level combinational logic, sequential logic(RT-level), custom purpose processor design(RT -level), optimizing custom single purpose processors.

UNIT II: GENERAL PURPOSE PROCESSORS

Basic architecture, operations, programmer's view, development environment, Application specific Instruction -Set processors (ASIPs)-Micro controllers and Digital signal processors.

UNIT III: STATE MACHINE AND CONCURRENT PROCESS MODELS

Introduction, models Vs Languages, finite state machines with data path model(FSMD),using state machines, program state machine model(PSM, concurrent process model, concurrent processes, communication among processes, synchronization among processes, Implementation, data flow model, real-time systems.

UNIT IV: COMMUNICATION PROCESSES

Need for communication interfaces, RS232/UART, RS422/RS485,USB, Infrared, IEEE1394 Firewire, Ethernet, IEEE 802.11, Blue tooth.

UNIT V: EMBEDDED/RTOS CONCEPTS-I

Architecture of the Kernel, Tasks and task scheduler, interrupt service routines, Semaphores, Mutex.

UNIT VI: EMBEDDED/RTOS CONCEPTS-II

Mailboxes, Message Queues, Event Registers, Pipes-Signals.

UNIT VII: EMBEDDED/RTOS OCNCEPTS-III

Timers-Memory Management-Priority inversion problem-embedded operating systems-Embedded Linux-Real-time operating systems-RT Linux-Handheld operating systems-Windows CE.

UNIT VIII: DESIGN TECHNOLOGY

Introduction, Automation, Synthesis, parallel evolution of compilation and synthesis, Logic synthesis, RT synthesis, Behavioral Synthesis, Systems Synthesis and Hard ware/Software Co-Design, Verification, Hardware/Software co-simulation, Reuse of intellectual property codes.

TEXT BOOKS

1. Embedded System Design-A Unified Hardware/Software Introduction- Frank Vahid, Tony D.Givargis, John Wiley & Sons, Inc.2002.
2. Embedded/Real Time Systems- KVKK prased, Dreamtech press-2005.
3. Introduction to Embedded Systems - Raj Kamal, TMS-2002.

REFERENCE BOOKS

1. Embedded Microcomputer Systems-Jonathan W.Valvano, Books/Cole,Thomson Learning.
2. An Embedded Software Primer- David E.Simon, pearson Ed.2005

SYSTEM MODELLING & SIMULATION

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II

SIMULATION SOFTWARE:

Comparison of simulation packages with Programming Languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III

BUILDING SIMULATION MODELS:

Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT IV

MODELING TIME DRIVEN SYSTEMS:

Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation.

UNIT V

EXOGENOUS SIGNALS AND EVENTS:

Disturbance signals, state machines, petri nets & analysis, System encapsulation.

UNIT VI

MARKOV PROCESS

Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous – Time Markov processes.

UNIT VII

EVEN DRIVEN MODELS:

Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.

UNIT VIII

SYSTEM OPTIMIZATION:

System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

TEXT BOOKS:

1. System Modeling & Simulation, An introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003

REFERENCE BOOKS:

Systems Simulation – Geoffrey Gordon, PHI, 1978

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

(ELECTIVE IV)

UNIT –I

Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA – Features, Architectures, Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT-II

CPLDs: Complex Programmable Logic Devices: Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1 to 5), Cypress FLASH 370 Device technology, Lattice pLSI's architectures – 3000 series – Speed performance and in system programmability.

UNIT – III

FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT-IV

Finite State Machines (FSM): Top Down Design, State Transition Table , State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.

UNIT-V

FSM Architectures: Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One_Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.

UNIT- VI

Design Methods: One –hot design method, Use of ASMs in one-hot design method, Applications of one-hot design method, Extended Petri-nets for parallel controllers, Meta Stability, Synchronization, Complex design using shift registers.

UNIT-VII

System Level Design: Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool (FPGA Advantage), Design flow using CPLDs and FPGAs.

UNIT - VIII

Case studies: Design considerations using CPLDs and FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.
3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.

MIXED SIGNAL SIMULATION LABORATORY

By considering suitable complexity Mixed-Signal application based circuits (circuits consisting of both analog and digital parts), the students are required to perform the following aspects using necessary software tools.

- Analog Circuits Simulation using Spice Software.
- Digital Circuits Simulation using Xilinx Software.
- Mixed Signal Simulation Using Mixed Signal Simulators.
- Layout Extraction for Analog & Mixed Signal Circuits.
- Parasitic Values Estimation from Layout.
- Layout Vs Schematic.
- Net List Extraction.
- Design Rule Checks.
