MEMORANDUM OF UNDERSTANDING (MoU)

between

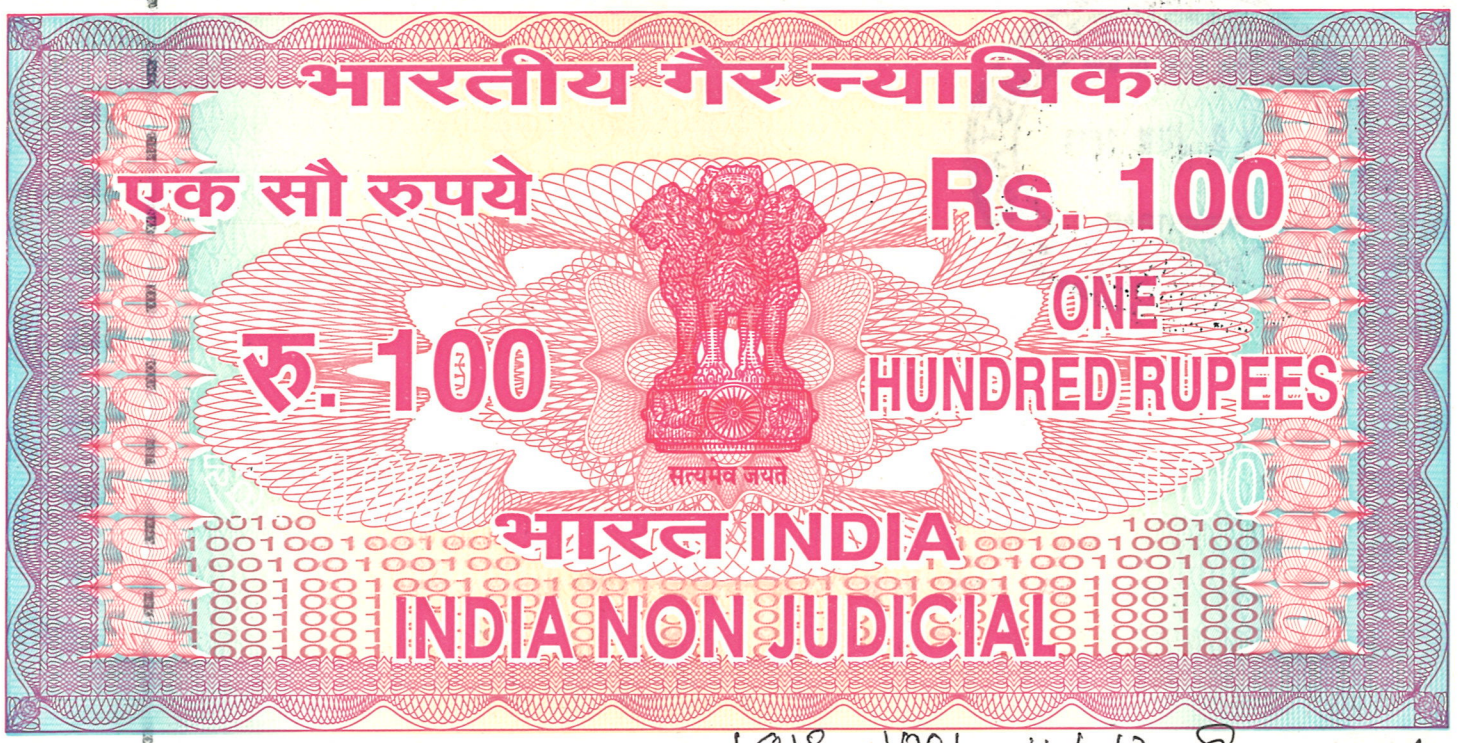
National Programme on Technology Enhanced Learning (NPTEL), IIT Madras

Seer Academi
USA, Banglore and Hyderabad.

and

Jawaharlal Nehru Technological University Kakinada
Kakinada - 533 003. Andhra Pradesh, India

12th June, 2013



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Registrar JNTUK Kakinada

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MoU to Collaborate on ESDM Manpower Development

This Memorandum of Understanding is hereby undertaken between Jawaharlal Nehru Technological University, Kakinada(University), IIT Madras (NPTEL)and Seer Akademi (Seer), henceforth known collectively as the Parties, on the 12th day of June, 2013 at JNTUK Kakinada. The Parties hereby propose to setup a collaborative **Center for ESDM Manpower development under the University**that has the objective of creating industry oriented programs, large capacity manpower development using modern technology, rapid induction of technological trends into curriculum, focus on Washington Accord compatibility and means to facilitate the participation of industry experts in the training of students and faculty.

Context

The Central government has called for massive capacity building in educational institutions in the ESDM sector – 28 Million workers to be trained by 2020 (Placeholder1). Accordingly, many states, including Andhra Pradesh have formulated their own policies to promote industry development and manpower development.Approximately, 1 Million (10 lakhs) workers are supposed to be in the white collar classification which implies that we must make efforts collectively to utilize every graduating engineer to

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his/her full potential. In addition, 2500 PhDs per year in this sector are called for, however, the Nation lacks means to attract and supervise talented individuals to join PhD programs. Whereas current programs are restricted in intake capacity, we need to envisage and implement methods to regulate and train large numbers of students using modern technology. Kindly refer to the National Policy on Electronics – 2012 for further information.

Reference Model

As technology evolves, we find that both curriculum and methodology of teaching need to be changed. Specifically, in the Indian Context, expertise is this sector is to be found in the industry, which is based in Silicon Valley, Bangalore and Hyderabad. The following models are cited as functional, successful methodologies to be adopted.

1. The M.S. in VLSI/Embedded Systems programme at JNTUH , run under an MOU with Seer Akademi is a reference model for PPP programs
2. Seer Akademi's patent-pending online + local model is used as a reference to train large numbers at once with academic rigor.
3. Massive Open Online Course Initiatives such as EdX (MIT), Coursera (Stanford) and upcoming startups like Udacity.
4. EPub Technology from multiple global vendors that makes digital books, workbooks, exams available and feasible.
5. Shared Physical laboratories such as the Stanford Nano Technology Laboratory, UC Berkeley's Laboratories and San Jose State University Wafer Fabrication Facility.
6. Engineering Doctorate programs for working professionals offered in the UK and other EU nations.
7. Recent reforms at IITs with respect to B.Tech and M.Tech projects and options to substitute them with course credits.

Collaboration

1. Seer Akademi, in collaboration with industry participants shall form a Center for ESDM studies which offer programs similar to the current reference models cited but extending to other disciplines within the ESDM sector.
    a. ESDM verticals are as identified below and by the Department of Electronics and Information Technology.
        i. VLSI, Embedded Systems, Computer Science (Product Design focus), Information Technology Infrastructure, Telecommunications and Solar PV engineering are thrust areas
    b. The ESDM center shall aspire to be facility of national and international prominence along the lines of ITRI, Taiwan and IMEC, Belgium.
2. University and Center participants shall setup processes and mechanisms to train a large volume of students in cutting edge ESDM skills

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3. The parties collectively seek to establish a reference model of laboratory infrastructure and curriculum using the help experts from industry/academia.
    a. Within each ESDM segment/specialization, industry participants shall form a sub-committee which meets every 6 months to formulate, modify and ratify curriculum. This is needed in order to keep up with the rapidly changing trends in technology and market requirements.
    b. Refer to Operating procedures document for further details.
4. As in the reference model, experts from the industry will be invited to deliver instruction in their domain of expertise/practice. Industry participants seek to contribute/refer qualified instructors for this purpose.
5. NPTEL will fund the development of the courses for programs approved by University's Academic Section. Courses once developed and recorded will become the Intellectual Property of NPTEL.
    a. Seer shall facilitate recording of NPTEL content for approved programs using its Silicon Valley, Hyderabad and Bangalore offices as applicable.
6. The Center may initiate relationships with universities and laboratories in India and abroad to offer courses, exchange programs and laboratory facilities to its students.
7. The benefits of this center may extend to Undergraduate programs by incorporating key electives and core subjects into B.Tech programs.
8. If feasible, University and Seer Akademi seek to serve as a Talent Magnet for PhD candidates from industry by creating a model EngD program with the following objectives and as further documented later in this proposal.
    a. Promote research in ESDM inter-disciplinary fields and propagate into curriculum.
    b. Create an instructor pool for the benefit of the entire University community
    c. Create a mentoring relationship between industry leaders and full time students.
9. A Technical Advisory Board consisting of Industry experts and academic experts shall be constituted. The Vice-Chancellor of University may nominate a qualified University representative in consultation with other Advisory Board Members to this Board for Academic oversight. The term of such a representative shall be 12 months.
10. Fees and Revenue sharing
    a. The fee structure shall be set in a dynamic fashion which accomplishes the following:
        i. Allow a student to finish a base set of courses towards a degree objective at a predictable fee.[BASE FEE]
        ii. Allow industries, laboratories and external bodies to offer modules and electives for credit at a fee proportionate to their investment. Such electives and modules must be approved by the curriculum sub-committee.[THIRD PARTY FEE]. Unless declared at the time of admission, such external courses must only be deemed electives and suitable in-house options must be available.
        iii. Students shall be allowed to attend lectures from anywhere, but laboratories will be at the appropriate centers in Hyderabad/Bangalore or third party facilities.
    b. BASE FEE shall be apportioned as follows:

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i. A fixed infrastructure fee towards hardware, software and technology costs in the amount of INR TBD per student per semester, payable directly to vendors such as Cisco, Synopsys/Cadence/Mentor, ARM, VMWARE etc.
ii. A fee of INR 35,000 per student per semester to be shared by the parties as follows
    1. 15% to University
    2. 5% for Faculty Development Programs to University.
    3. 5% for research grants, conferences, publications etc. to Seer Akademi.
    4. 75% to Seer Akademi

c. THIRD PARTY FEE is paid directly to provider. Students are under no obligation to take such courses/material unless declared to them prior to admission as a core course or as required material. This is only a mechanism to allow students to take advanced electives and access lab facilities not available at universities.
d. MOU programs with foreign universities or lab facilities will be subject to variation because of other costs involved and also due to fluctuations in currency rates.
e. The parties shall create an escrow mechanism at a reputed bank for revenue collection and disbursal. Additionally, an external statutory audit shall certify compliance annually to set policies for revenue sharing.
f. Shared costs such as advertisements, events, visiting faculty hospitality, audit and escrow functions etc. shall be shared by all parties in a pro-rata manner according to their share of the revenue.
g. NPTEL funding of courses: University and Seer seek to put lecture content in the public domain and make the courses affordable even further. Hence, they will apply to NPTEL for funding of lecture development. NPTEL will pay the University for development of ESDM courseware for these programs, which in turn shall pass on the revenue to Seer through the Escrow account mechanism within 5 business days
h. NPTEL funding of collateral: All courses shall have collateral such as assignments and sample projects. This material is time-bound and needs to be updated on an annual basis. Any updates to courses shall also be undertaken annually.

11. Capacity
    a. The center shall aim to serve its mandate as follows (optimal use of technology, scheduling and timesharing of facility will be done to reduce infrastructure costs)
        i. 25 Students in VLSI Design for academic year 2013-2014
        ii. Further expansion to other programs and disciplines to be determined subsequently.
    b. The center shall conduct faculty training for University and affiliated colleges – Upto 300 faculty members shall be trained annually.Participants shall be charged a nominal fee.
    c. If feasible, the center shall run Talent Magnet programs for experienced engineers to acquire PhDs with the following targets and according to the Engineering Doctorate guidelines.
        i. 50 candidates in academic year 2013-2014
        ii. 125 candidates in academic year 2014-2015

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iii. 200 candidates in academic year 2015-2016

12. Extension to other disciplines
    a. The Parties seek to extend the benefits of Seer Akademi's technology to non ESDM disciplines by establishing Global classrooms and teaching services from reputed institutions in India and abroad.
13. Other infrastructure
    a. University may run the program at its constituent colleges and any of its affiliated colleges and Seer offices. Students of this MOU based programs shall have the same responsibilities and privileges as any other student at the respective campuses, including but not limited to use of hostels, libraries, placement services, logistics etc.
14. Term and Termination
    a. The MOU shall have a term of 7 years, given the long term perspective of academic engagements.
    b. Either party may terminate the program by giving a written notice to the other : all academic obligations to enrolled students shall be completed and fresh admissions suspended in such a case.
    c. Parties shall refer the matter to a neutral arbitrator in case of an irreconcilable dispute. Such Arbitrator will be in the jurisdiction of Hyderabad, Andhra Pradesh.
15. Liability
    a. Other than duly accrued fees, neither party shall have any liability to the other. As mentioned earlier, all disputes, if irreconcilable, shall be referred to a neutral arbitrator in the jurisdiction of Hyderabad, Andhra Pradesh.

Signatories

JNTUK Kakinada :

Name :

Title :

Signature and/or Seal

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA ★ REGISTRAR'S OFFICE ★

NPTEL, IIT Madras:

Name : K. MANGALA SUNDER.

Title: National Web Courses Coordinator, NPTEL Project, MHRD.

Signature and/or Seal

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Co-ordinator, NPTEL, CCE
IIT Madras, Chennai 600 036

Seer Akademi :

Name :

Title: SRIKANTH JADCHERLA
CEO

Signature and/or Seal

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ANNEXURES

SEER AKADEMI PVT.LTD.
M.Tech (VLSI)

COURSE STRUCTURE AND SYLLABUS

I Semester (Duration 20 weeks)

Code	Subject	L	P	Credits
-	Computer Architecture / Computational Methods	3	3	3+2
-	Data Structures&Algorithms for VLSI	3	3	3+2
-	Linux, Perl and Python	3	3	3+2
-	Digital VLSI Design 1 - Frontend	3	3	3+2
-	**Total Credits**	12	12	**20**

II Semester (Duration 20 weeks)

Code	Subject	L	P	Credits
-	Digital VLSI Design 2 - Backend	3	3	3+2
-	Advanced Verification using System Verilog	3	3	3+2
-	DSP / FPGA based emulation/system development (For VLSI)	3	3	3+2
-	Protocols & Interfaces with Verification Methodology using UVM	3	3	3+2
-	Semiconductor Devices	0	3	2
-	Seminar	0	0	2
	Total Credits	12	12	**24**

III Semester (Duration 20 weeks)

Code	Subject	L	P	Credits
-	Advanced Physical Design / Std cell library design	3	3	3+2
-	Low Power design lab	0	3	2
-	Project – Phase I/Internship	-	-	17
	Research Methodology (University Provided Audit course)	-	-	-
	Total Credits	6	6	**24**

IV Semester(Duration 20 weeks)

Code	Subject	L	P	Credits
-	Project Phase 2/Internship	-	-	22
	Total Credits	-	-	**22**

Distribution of Credits

Subject	L	P	Credits
1st Semester	12	12	20
2nd Semester	12	15	24
3rd Semester	3	6	24
4th Semester	-	-	22
G. Total	**30**	**33**	**90**

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M.Tech (VLSI)

Computer Architecture

Objective:

The main objectives of the course are

- To study the modern computer organization by following the examples of Pentium 4, Itanium 2, OpenSPARC T1 and T2, PowerPC and ARM processors
- To study the virtual memory (paged and segmented) and multilevel cache memory organization.
- To study the organization of instruction pipelining.
- To study the methods of input/output organization

Lecture:

UNIT I - Introduction &Performance measurement in computer architecture

Basic concepts of computer organization. The stored program model. Classes of computer architecture. Processor vs. System architecture. Elements of computer systems – processors, memories, I/Os, disks, buses etc.
Goals of computer architecture – performance, throughput, latency, power, cost. Processor performance vs. system performance. Comparison of various platforms in terms of performance and efficiency.

UNIT II- Processor Architecture

Internal elements and architecture of processors. Instruction execution. Instruction set architectures, CISC vs. RISC architectures. Bus architecture. Multi Processor architecture. Memories and Caches. Cache coherency. Pipelining and data path elements.

UNIT III - System and System on Chip architecture

System architecture elements. H/W component selection and datasheet analysis. Bill of Materials. IP selection and System on Chip integration. Standard interfaces and I/Os. Analog and Mixed signal element integration. Reset and clocking elements. Multi processor system.

UNIT IV - Special processor/system architecutes

Application specific processors. Packet processing. Microcontrollers. Network controllers. DSP and Multimedia processors. GPU elements.

UNIT V - Current Architectural survey

An overview of the latest Intel, ARM, TI, SPARC and Power PC architectures as modern SOC architectural elements.

Lab :

Tools used during laboratory works: Linux, Perl, Gcc,Gdb.

- Study and implementation of processor performance using opencores.
- Study and implementation of performance of openSPARC and ARM / ARC processors.
- Study and implementation of SOC architectures

Course Project:

A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.

Course Material:

The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latestresearch, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

- V.C. Hamacher, Z.G. Vranesic, S.G. Zaky. "Computer Organization". 5th Edition. "Peter", 2003. 832p.
- David A. Patterson and John L. Hennessy. Computer Organization and Design, Revised Printing, Third Edition, Third Edition: The Hardware/Software Interface (The Morgan Kaufmann Series in Computer. Series in Computer Architecture and Design). Morgan Kaufmann; 3rd Edition. 2007. 741p.
- Andrew S. Tanenbaum. Structured Computer Organization Prentice Hall; 5th Edition. 2005. 800p.
- W. Stallings. "Computer Organization and Architecture. Designing and Performance". 7th Edition. Prentice Hall. 2005. 792p.
- J.L. Hennessy, D.A. Patterson. "Computer architecture: A Quantitative Approach", 4th Edition. Morgan Kaufmann, 2006. 704p.
- UltraSPARC T1™ Supplement to the UltraSPARC Architecture 2005. Sun Microsystems. 2006
- OpenSPARC™ T2 Core Microarchitecture Specification. Sun Microsystems. 2008

Data Structures/ Algorithms

Objective of the Course

The course emphasizes programming methodology, procedural abstraction, and in-depth study of algorithms, data structures, and data abstractions. It also aims to introduce basic data types, data structures, types of data structures - Linear and Non-Linear data structure, representation of stack, queue and linked list; complexity and efficiency of various types of sorting and searching techniques; applications of data structures
At the end of the course, the student will understand:

- Data Structures
- Analysis techniques.
- Linear data Structure like array, stack, queue and linked list.
- Non-linear data structure like tree and graphs.
- Sorting and Searching methods

Outline of Course
Lectures = 40hrs
Practical/Tutorials = 80hrs
Total = 120hrs

Detailed Syllabus

UNIT I - Introduction 5 Hrs.

Algorithms, Data Structures, Summation Formulas and properties, Sets, Relations, Functions, Graphs, Trees, Counting, Probability Concepts.Object-Oriented Design Principles, Encapsulation, Inheritance, Polymorphism, Basic goals andconcepts of C++/Java, Programming Skills, Xtreme Programming, debugging, testing, Application ofOO concepts.

UNIT II - Elementary Data Structures 5 Hrs.

Introduction of Stack, Queue and Linked List, Application of Stacks and Queue, Representationof Queue and its types, Representation of Linked List and its types, Priority Queue,Implementing Objects, Linked List, Stack, Queue.

UNIT III - Recursion and Trees 10 Hrs.

Characteristic of recursive Methods, Efficiency of Recursive methods, Tower of Hanoi Example,Eliminating Recursion, Applications of Recursion.The Tree Abstract Data Type, Basic Algorithms on Trees, Types of trees and algorithms, BinarySearch Tree.

UNIT IV - Graphs and strings 10 hrs

The Graph Abstract Data Type, Data Structures for Graphs, Graph Traversal: BFS and DFS ofDirected and Undirected Graph, Connected Components, Spanning Trees, Bi- connected Components and DFS. The String Abstract Data Type, Brute-Force String Pattern Matching, Regular ExpressionPattern Matching, Tries.

UNIT V - Sorting and Searching Methods 10 Hrs.

Introduction to Sorting Techniques: Insertion Sort, Selection Sort, Bubble Sort, Heap Sort, QuickSort, Merge Sort, Radix Sort, Analysis of Efficiency and Complexity of Sorting of various cases(Best, Average and Worst.

Course Project:

A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.

Course Material:

The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

RECOMMENDED BOOKS (*)

MAIN READING

1. Jean-Paul Tremblay and Paul G, "An Introduction to Data Structures with Applications", Sorenson Publisher – Tata McGraw Hill.
2. Wiley Higher Education, "Data Structures and Algorithms in Java", 3rd Edition, John Wiley & Sons.

SUPPLEMENTARY READING

1. Michael T. Goodrich and Robert Tamassia, "Data Structures and Algorithms in Java", John Wiley Publication
2. Robert Lafore, "Data Structures and Algorithms in Java", 2nd Edition, Pearson Education.

(*) Latest edition of the books need to be procured.

Linux, Perl and Python

Objective:

Be able to analyze problem specifications, design, develop and deliver programs in the domain of Linux, Perl and Python.

Format:

This course is offered in a hands-on manner where certain skills are to be acquired by the candidate. Lectures are mostly intended to in the format of demo/tutorials in accordance with modern pedagogy. The student is given a series of small-medium scale assignments and projects which must be performed on their own.

Textbook:

1. An online compilation of references will be published to the student

2. A current print edition will be recommended based on availability in India

3. Content in this sphere is rapidly changing – Instructor will 'push' electronic content to students

References:

Instructor will publish an updated list of references throughout the course since material is rapidly changing

Digital VLSI Design I - Frontend

Objective:

The study of IC design basics, levels, strategies, options, methods, styles, challenges, economics and trends especially front-end.In the process of the laboratory work it is necessary to study the main front-end IC design tools and to implement in the basic digital electronic circuits design.

Lecture:

UNIT I - Introduction -Levels of IC design – Digital circuit fundamentals

Concept of IC. IC structure, components, applications. History and evolution of the IC industry.Moore's Law. Design economics - Nonrecurring engineering costs (NRE) & Recurring costs, Yield & Technology scaling.

System level Design. Top down design.Bottom up design. Back end design. Design abstraction levels. Behavior Level.Register-Transfer Level (RTL).Logic Level.Circuit Level.Component level.Examples of Domains and its Abstraction Levels.

CMOS logic gates, Combinational circuits, Sequential circuits, FSM

UNIT II - Design Flow

Design flow: Frontend –Marketing Requirements, Design specification, Verification plan, RTL description, Functional verification, Synthesis. Backend – Partitioning, Floor planning, Placement, CTS, Routing & layout generation, layout verification, Tapeout. Foundry - Fabrication

Introduction to Testing – Need for testing, manufacturing test, design for test, chip-level test, system-level test, test generation & fault models

Introduction to System on chip (Soc) design - Soft cores, Firm cores, Hard cores.Study of AMBA AXI4 protocol.

UNIT III - IC Design techniques & options, CAD design, Design challenges

Structured design techniques: hierarchy, regularity, modularity, locality.

Design options: Programmable logic Design, sea of gates and gate array design, standard cell design, full-custom design.Study of FPGA tools.

Using of CAD tools: Behavioral synthesis tool, RTL synthesis tool , logic optimization tool, structural to layout synthesis tool, layout synthesis tool, design capture tools, design verification tools, circuit extractor, design rule checker (DRC), electrical rule checker (ERC), layout vs. schematic.

Design challenges –

Microscopic issues: ultra-high speeds, power dissipation, supply rail drop, importance of interconnect, noise, crosstalk, reliability, manufacturability, clock distribution.
Macroscopic issues: time to market, design complexity, high levels of abstractions, reuse, IP, portability, tool interoperability.
Sub-nm technologies: technology scaling, switching power reduction, leakage power control, process variations, die to die frequency variation, temperature variation.

UNIT IV- Digital Design and Synthesis

Verilog HDL. Concepts of Design planning, RTL design for Sequential & combinational circuits, State machines design & encoding.Simulation , waveform generation, coverage reports.

Synthesis concepts, Technology libraries, Constraints, Netlist generation & optimization.

UNIT IV – Design verification using System Verilog & VMM

System Verilog – Verification guidelines, Data types, Interfaces, Assertions, Randomization, Coverage

Concepts of verification, verification plan, test cases &testbench generation

VMM – Layered test bench architecture: Signal, Command, Functional, Scenario & Test layers

Lab:

Tools used during laboratory works: VCS &Design Compiler

- Study and implementation using VCS and Design Compiler

Course Project:

A project of suitable complexity, comprising of RTL design, Testbench formation and coverage must be completed by the student.

Course Material:

The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latestresearch, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

- Synopsys recommended course material and lectures.
- N. Weste, K. Eshragyan. Principles of CMOS VLSI Design. Adisson Wesley, 1993
- J.F. Wakerly. Digital Design - Principles & Practices, Prentice Hall, 2001
- Digital logic design by Morris Mano
- Verilog HDL: A guide to digital design & synthesis, 2e by Samir Palnitkar
- System Verilog for verification, 2e by Chris Spear – Springer
- IEEE Std 1364™-2005 - Verilog LRM
- System Verilog LRM
- System Verilog Golden reference guide

Digital VLSI Design II - Backend

Objective:

The study of IC design basics, levels, strategies, options, implementation methods, styles, challenges, and trends especially back-end.

In the process of the laboratory work it is necessary to study the main IC design tools and to implement the basic digital electronic circuits' design flow.

Lecture:

UNITI–Recap of Front-end flowand Logic Synthesis.

Recap Units II and IV of Course Digital VLSI Design I – Front-end.

UNITII –Physical Design Setupand Floorplanning

VLSI Design Cycle, Methodology of Physical Design, Simplified Cycle of Physical IC Design, Partitioning, Floorplanning, Placement, Routing, Compaction, Verification. Logical libraries, Physical Libraries, Timing Constraints, Database format, Logical data setup, Physical data setup, Technology Files, Interconnect delay models, tcl scripting for automation.
Hierarchical Design Planning Flow, Pad Creation and Order Assignments, Core Area, Initializing the Floorplan, Timing Driven Placement, Placement with Hierarchical Gravity, Analyze placement and Color Modules, Post-initialization Macro placement controls, Large Macro Handling, Power Network Synthesis (PNS), Power Network Analysis (PNA).

UNITIII - Placement

Placement Methodology, Fast Iteration with Coarse Placement, Understanding the Congestion Calculation, Textual Congestion Report, Analyzing the Congestion Map, Global Route (GR) for Congestion Map, Strategies for Fixing Congestion Problems, Congestion-Driven Placement Options, Adjusting Cell Density, Timing and Power Optimization for Best QoR, Congestion-Driven Placement, Incremental Congestion Refinement, Refinement Flow, Incremental mode, Area Recovery, Timing Analysis.

UNITIV–Clock Tree Synthesis

Design Status, Start of CTS Phase, Clock Tree Synthesis, CTS Goals, Define Clock Root Attributes, Stop, Float and Exclude Pins, Generated and Gated Clocks , User-defined or Explicit Stop Pins, Defining an Explicit Float Pin, Preserving Pre-Existing Clock Trees, Impact of Preexisting Clock Cells, Logical Design Rule Constraints, Non-Default Clock Routing, Specifying Non-Default Rules, Nondefault Rule Options, Effects of Clock Tree Synthesis, Incremental Placement / Optimization, Analysis using the CTS GUI , Clock Tree Optimization, Inter-Clock Delay Balancing, Post Route CTO.

UNITV–Routing and Post Tapeout flow

Design Status, Start of Routing Phase, Grid-Based Routing System, Routing over Macros, Pre-Route Checks, Routing Operations, Core Routing Strategy, Fixing DRC Violations, Crosstalk-Induced Noise, Crosstalk-Induced Delay, Crosstalk Prevention, Crosstalk Correction, Wire Sizing.

Labs:

Tools used during laboratory works: Design Compiler and IC Compiler.

Course Project:

A project of suitable complexity, comprising of RTL coding, Synthesis and complete netlist to GDSII flow must be completed.

Course Material:

The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latestresearch, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

- Synopsys recommended course material and lectures.
- J.P. Uyenmura. Introduction to VLSI Circuits and Systems, J.Wiley & Sons, 2002.
- J.M. Rabaey, A. Chandrakasan, B. Nikolic. Digital Integrated Circuits - A Design Perspective, Prentice Hall, 2003.
- J.P. Uyenmura. Modern VLSI Design – System-on-Chip Design, Prentice-Hall, 2002.

Advanced verification using system verilog

Objective:
Be able to analyze problem specifications, design, develop and deliver programs in the domain of advanced system verilog.

Format:
This course is offered in a hands-on manner where certain skills are to be acquired by the candidate. Lectures are mostly intended to in the format of demo/tutorials in accordance with modern pedagogy. The student is given a series of small-medium scale assignments and projects which must be performed on their own.

Textbook:

1. An online compilation of references will be published to the student

2. A current print edition will be recommended based on availability in India

3. Content in this sphere is rapidly changing – Instructor will 'push' electronic content to students

References:
Instructor will publish an updated list of references throughout the course since material is rapidly changing.

DSP

Objectives:

To develop skills for analyzing and synthesizing algorithms and systems that process discrete time signals, with emphasis on realization and implementation.

Outline of Course
Lectures = 40 hrs
Practical/Tutorials = 120 hrs
Total = 120 hrs

Detailed Syllabus

UNIT I – Introduction 5hrs

Signal Processing and its Applications, LTI, Discrete Time Fourier Transform, Symmetry properties of DTFT, Convergence of DTFT.

UNIT II – Sampling 5hrs

Sampling, Downsampling, Upsampling, Region of Convergence for Z.T., C.R.T.To Compute Inverse Z.T.

UNIT III – Systems 10 hrs

Difference Equations and LTI Systems, Realizations of L.C.C.D.E., Realizations of IIR Filters with Rational Transfer Function, Cascade + Parallel Implementation of ± IR Filters with Rational Transfer Function

UNIT IV – Filter Design 10 hrs

Realization of FIR Filters, Linear Phase Filtering, Conditions for Achieving Linear Phase, Filter Design, FIR Filter Design using Windows, Optimum FIR Filter Design, Algorithms for Optimal Filter Design, IIR Filter Design, IIR Filter Design Transformation,

UNIT V – Fourier Transformations 10 hrs

Discrete Fourier Series, and DFT = Discrete Fourier Transform, Properties of DFT, Using DFT to do Linear Convolution, Fast Fourier Transform, FFT: Decimation in Frequency, DCT and its Relation to DFT

Course Project:

A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.

Course Material:

The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will

decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

FPGA Bases Systems Development

Objective :

The main objective of the course is to introduce digital design techniques using field programmable gate arrays (FPGAs). This will be followed by discussing FPGA architecture, digital design flow using FPGAs, and other technologies associated with field programmable gate arrays. The course study will involve lab projects to give students hands-on experience on designing digital systems on FPGA platforms.

Outline of Course
Lectures = 40 hrs
Practical/Tutorials = 120 hrs
Total = 120 hrs

Detailed Syllabus

UNIT I : 5 hrs

Introduction to ASICs and FPGAs, Difference between ASICs, FPGAs and other programmable logic devices, Fundamentals in digital IC design, FPGA Programming Technologies, FPGA Logic Cell Structures, Basic FPGA technology (antifuse, RAM based etc)

UNIT II : 5 hrs

Basic FPGA Design Flow – Design Entry : VHDL, Time model (Elmore delay), Area model, Energy model, Synthesis, Clustering, Placement, Routing

UNIT III : 10 hrs

Optimization for FPGAs : Architecting Speed, Architecting Area, Architecting Power, Clock Domains, Synthesis, Optimization, Optimizing Physical Design, PCB issues

UNIT IV : 10 hrs

FPGA Programmable Interconnect and I/O Ports, FPGA Implementation of Combinational Circuits, FPGA Sequential Circuits, Timing Issues in FPGA Synchronous Circuits, Introduction to Verilog HDL and FPGA Design flow with using Verilog HDL, FPGA Arithmetic Circuits

UNIT V : 10 hrs

FPGAs in DSP Applications, FPGA High-level Design Techniques, Programming FPGAs in Electronic Systems, Latest Trends in Programmable ASIC and System Design

Lab :

The lab work will focus on relevant FPGA tools and will require students to use FPGA technology to implement arithmetic circuits and for DSP applications.

Course Project:

A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.

Course Material:

The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References :

- Wayne Wolf, "FPGA-Based System Design," Prentice Hall, 2004
- Steve Kilts, "Advanced FPGA Design," Wiley Inter-Science,
- Xilinx User Manuals and Application Notes

Protocols and Interfaces

Objective:

The study of architectural elements, performance metrics and system architecture of computer systems with a focus on interfaces and protocols.

In the process of the laboratory work it is necessary to use and study standard and emerging architectures.

Lecture:

UNIT I - Introduction (Recap)

Basic concepts of computer organization.The stored program model.Classes of computer architecture.Processor vs. System architecture.Elements of computer systems – processors, memories, I/Os, disks, buses etc.

UNIT II - Data Processing in Microcontrollers

Programs based on data transfer, arithmetical, logical, branching, bit (Boolean) operation instructions.

UNIT III - Organization communications of Microcontroller with the object of control

Data Transfers between On-chip hardware Microcontroller and peripheral Units. Signal processing and conditioning.Timing Function conditioning.Software conversion of codes.Software support of A/D and D/A Converters.

UNIT IV - Interfacing with Microprocessor Systems

Organization communications of Operator with Microcontroller.Keyboard and Display interfacing. Input/ output enhancement mode

UNIT V- Protocols

Types of memory interfaces – SRAM, DRAM, Flash, EPROM/ROM and corresponding protocols.
Types of Disk protocols – SATA, IDE, SCSI
Special memories – Video RAMs, RDRAM, CAM
Interrupt controllers, priorities and arbitration. ISRs and context saving architectures.
Programmable interrupt controller
PCI, USB, 1394, Ethernet, 802.11x, PCI Express, ACPI
Bridge functions
Storage area networks and protocols

Labs :

Tools used during laboratory works: Linux, Perl, Gcc,Gdb, VCS

- Study and implementation of interfacing exercises.
- Study and implementation of performance of memory systems and their impact on system performance
- Study and implementation of Standardinterfaces

Course Project:

A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.

Semiconductor Devices Lab

Objective:
Be able to analyze problem specifications, design, develop and deliver programs in the domain of semiconductor devices.

Format:
This course is offered in a hands-on manner where certain skills are to be acquired by the candidate. Lectures are mostly intended to in the format of demo/tutorials in accordance with modern pedagogy. The student is given a series of small-medium scale assignments and projects which must be performed on their own.

Textbook:

1. An online compilation of references will be published to the student

2. A current print edition will be recommended based on availability in India

3. Content in this sphere is rapidly changing – Instructor will 'push' electronic content to students

References:
Instructor will publish an updated list of references throughout the course since material is rapidly changing.

Advanced physical design

Objective:
Be able to analyze problem specifications, design, develop and deliver programs in the domain of advanced physical design.

Format:
This course is offered in a hands-on manner where certain skills are to be acquired by the candidate. Lectures are mostly intended to in the format of demo/tutorials in accordance with modern pedagogy. The student is given a series of small-medium scale assignments and projects which must be performed on their own.

Textbook:

1. An online compilation of references will be published to the student

2. A current print edition will be recommended based on availability in India

3. Content in this sphere is rapidly changing – Instructor will 'push' electronic content to students

References:
Instructor will publish an updated list of references throughout the course since material is rapidly changing.

Standard Cell Library Design

Objective:

The study of IC standard cell elements, memory types, memory failures, memory and cell characterization and testing.
In the process of the laboratory work it is necessary to study the main IC design tools and to implement electronic circuits in the form of standard cells and memories.
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Lecture:

UNIT I– Introduction

IC design flows. Use of standard cell elements vs. custom design and Gate array paradigms.Introduction to memory types and construction of memory elements.

UNIT II - Standard cell library composition and usage

Types of standard cell elements.Logical and functional elements, primitives and complex macros. Sequential elements and register files. (Flip flop and latch design). Data path elements.Library size vs. usage in standard flows. Drive strength and cell families. Layout of library elements – single height, double height cells. Power Management cells.

UNIT III - Standard cell characterization

Usage of standard cells by various tools. Information needed at each stage of design flow. Characterization parameters, setup and runs across PVT corners. Library representation formats. (Gate level simulation, synthesis, timing, layout, timing, LVS, DRC)

UNIT IV - Memory elements and array design.

Volatile and Non-volatile RAM, ROM,EPROM, Flash (EEPROM), OTP elements and cell design. State retention volatile memories. Array design – architecture, bitline/wordline optimization, sense-amps and mux/demux architecture. Memory banking, refresh cycle management. Multi-port memories.Cache memories.Special memories such as CAMs.

UNIT V– Memory defects, failures and testing, layout and characterization

Memory defects and repair.Temporal failures, Soft errors.Membist and other test techniques for memories.

Memory layout and its impact on performance.Characterization of memories – timing, area, power parameters. Layout views – hard macro representation, keep outs and congestion impact.

Lab :

Tools used during laboratory works: EDA tools using Synopsys EDK 90nm library.

- Study and implementation of standard cell library element
- Study and implementation of small register file from standard cell
- Study and implementation of memory element (SRAM 6 T cell)
- Study and implementation of memory array (SRAM)

Course Project:

A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.

Course Material:

The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latestresearch, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

- Synopsys, ARM, TSMC standard cell and memory library documentation
- Synopsys 90nm EDK library