

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
UNIVERSITY EXAMINATION CENTER, KAKINADA
M. TECH II SEMESTER (R13) - SPECIAL SUPPLEMENTARY EXAMINATIONS, SEPTEMBER - 2024

REVISED TIME TABLE

TIME: 02.00 PM TO 05.00 PM

BRANCHES	DATE & DAY		
	05-09-2024 (Thursday)	06-09-2024 (Friday)	09-09-2024 (Monday)
ECE			
Embedded Systems (55) VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN/VLSI & MICRO ELECTONICS (57/72/61/76)	Digital Signal Processors & Architectures Elective-III H6805	System on Chip Design H6806	Cad for VLSI H5701
Systems & Signal Processing/ Digital Image Processing/ Communication Engineering & Signal Processing/C&SP/IP (45,63,46,80,10)	Low Power VLSI Design H6809	--	--
VLSI&EMBEDED SYSTEMS/ EMBEDED SYSTEMS & VLSI /VLSID&ES/ES&VLSID (68,48,77,81)	CMOS Mixed Signal Circuit Design H6802	--	--
Digital Electronics & Communication Engineering/Digital Electronics And Communication Systems/ Electronics & Communication Engineering (37,38,70)	Embedded Real Time Operating Systems H6803		

- NOTE** i. ANY OMISSIONS OR CLASHES IN THIS TIME TABLE MAY PLEASE BE INFORMED TO THE CONTROLLER OF EXAMINATIONS IMEDIATELY. (0884-2300907)
 ii. EVEN IF GOVERNMENT DECLARES HOLIDAY ON ANY OF THE ABOVE DATES, THE EXAMINATIONS SHALL BE CONDUCTED AS USUAL.
 iii. THE CANDIDATES ARE REQUESTED TO INFORM THE UNIVERSITY ANY OTHER SUBSTITUTE SUBJECTS THAT ARE NOT INCLUDED IN THE ABOVE LIST IMMEDIATELY.

(All the above Examinations will be conducted at University College of Engineering, JNTUK, Kakinada only)
(The Hall Tickets will be placed at www.jntukexams.net)



Date: 02-09-2024

Controller of Examinations (PG)